Rev.3.0 Aug.29 2024

JSKT200&JSKH200

Description

1) A package of series of two chips.
2) With high thermal conductivity DBC as the insulation.
3) Welding by vacuum welding technology, which provide high reliability.

Typical Application

DC motor control, temperature control and light control system.

Absolute Maximum Ratings (Packaged into modules, unless otherwise specified, T_{CASE}=25℃)

Parameter	Test Conditions	Symbol	Values		Unit
			20	22	
Operating junction temperature range		T_j	-40~125		℃
Storage temperature range		T_{stg}	-40~125		℃
Repetitive peak off-state voltage	T_j=25℃	V_{DRM}	2000	2200	V
Repetitive peak reverse voltage	T_j=25℃	V_{RRM}	2000	2200	V
Non-repetitive peak off-state voltage	T_j=25℃	V_{DSM}	2100	2300	V
Non-repetitive peak reverse voltage	T_j=25℃	V_{RSM}	2100	2300	V
Average on-state current	T_C=85℃	$I_{T(AV)}/I_{F(AV)}$	200		A
Peak on-state surge current	t_P=10ms V_R=0.6V_{RRM}	I_{TSM}/I_{FSM}	5400		A
I^2t value for fusing	t_P=10ms V_R=0.6V_{RRM}	I^2t	145000		A^2s
Critical rate of rise of on-state current	I_G=2×I_{GT}	dI/dt	150		A/μs
Insulation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000		V

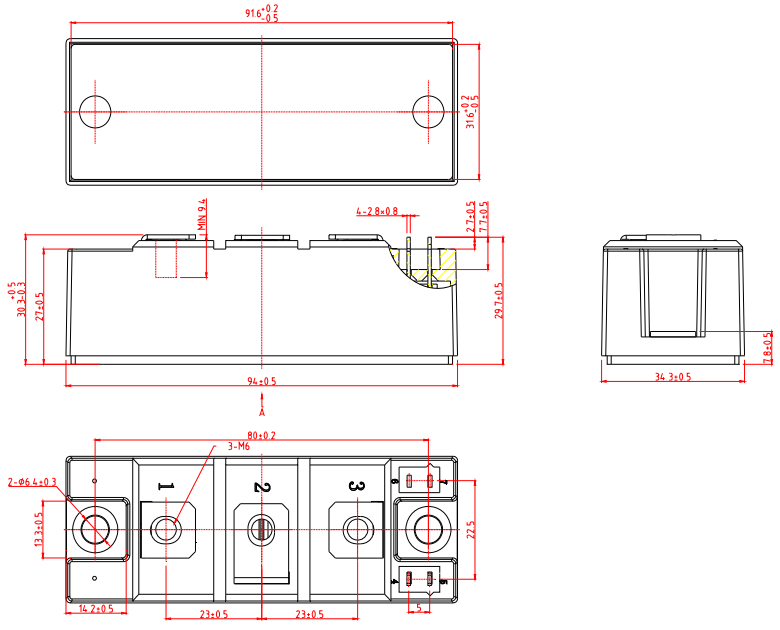
Electrical Characteristics (Packaged into modules, unless otherwise specified, T_{CASE}=25℃)

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	I_T=600A t_P=380μs	V_{TM}	≤1.8	V
Threshold voltage	T_j=125℃	V_{TO}	≤0.9	V
Dynamic resistance	T_j=125℃	R_d	≤1.6	mΩ

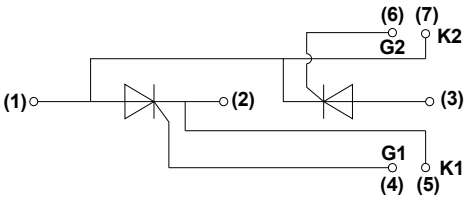
Repetitive peak off-state current	$V_D=V_{DRM}$ $T_C=25℃$ $T_C=125℃$	 I_{DRM1} I_{DRM2}	 ≤100 ≤60	 μA mA
Repetitive peak reverse current	$V_R=V_{RRM}$ $T_C=25℃$ $T_C=125℃$	 I_{RRM1} I_{RRM2}	 ≤100 ≤60	 μA mA
Triggering gate current	V_D=12V R_L=30Ω	I_{GT}	20-120	mA
Holding current	I_T=1A	I_H	≤250	mA
Latching current	I_G=1.2 I_{GT}	I_L	≤300	mA
Triggering gate voltage	V_D=12V R_L=30Ω	V_{GT}	≤1.8	V
Non triggering gate voltage	$V_D=V_{DRM}$ T_j=125℃	V_{GD}	≥0.25	V
Critical rate of rise of voltage	V_D=2/3V_{DRM} T_j=125℃ Gate Open	dv/dt	≥1000	V/μs
Thermal resistance	Junction to case Case to heatsink	$R_{th(j-c)}$ $R_{th(c-s)}$	0.12 0.08	℃/W

Mechanical Characteristics

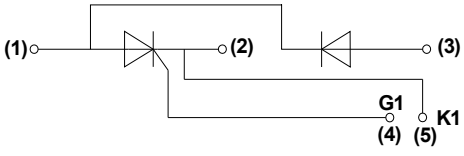
Module size	94mm×34.3mm
Module height	30.3mm
Terminal distance of (1) /(2) /(3)	23mm
Mounting torque(M5)	5±15%Nm
Terminal torque(M6)	5±15%Nm



T2



JSKT symbol



JSKH symbol

Instructions and Precautions

1) There is no severe vibration and shock in operating environment, and there should be no impurity and atmosphere which may corrode metal and damage the insulation in the air-dielectric.
2) The operating condition of the product can't out of range of the above parameters.
3) When the product is installed on the radiator, the radiator's surface should be confirmed flat, smooth, wipe clean with alcohol, and coated evenly with a layer of thermal grease which thickness is moderate on the contact surface between product and radiator. When the module is fastened on the surface of the radiator, the M5 or M6 screws and spring washers are used and fastened with 5NM torque. After the module is operated 1 hour, all screws must be refastened.
4) The connection with the main electrode of module can use copper, welding, socket and so on. The contact surface should be smooth and flat, which make good contact. While the connection with the control electrode of module is installed, attention should be paid to the corresponding connection of each pin. After the completion of the connection, do not plug and pull out the lead of the control electrode freely.

Ordering Information

JS KT 200 / 22

JieJie Semiconductor Co.,Ltd

KT: Thyristor module
KH: Thyristor and diode module

$I_{T(AV)}/I_{F(AV)}$=200A

20:V_{DSM}/V_{RSM}≥2100V
22:V_{DSM}/V_{RSM}≥2300V

Performance Curves

FIG.1: Power dissipation vs. on-state current (per thyristor or diode)

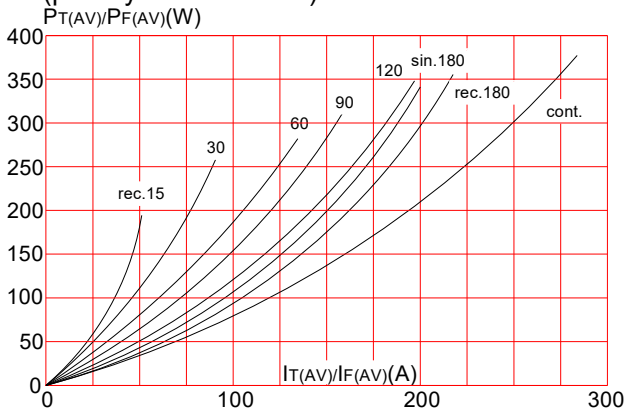


FIG.2: Maximum transient thermal impedance junction to case(per thyristor or diode)

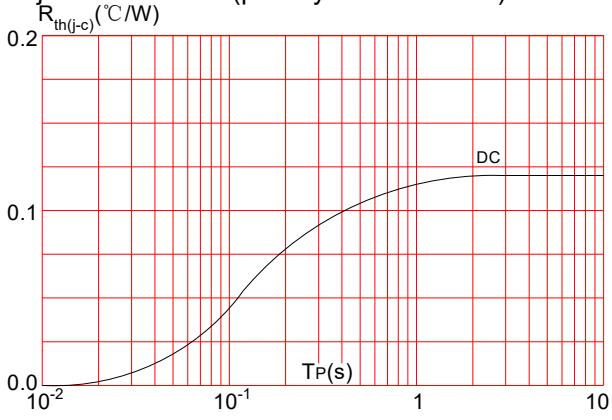


FIG.3: Forward characteristics
(per thyristor or diode)

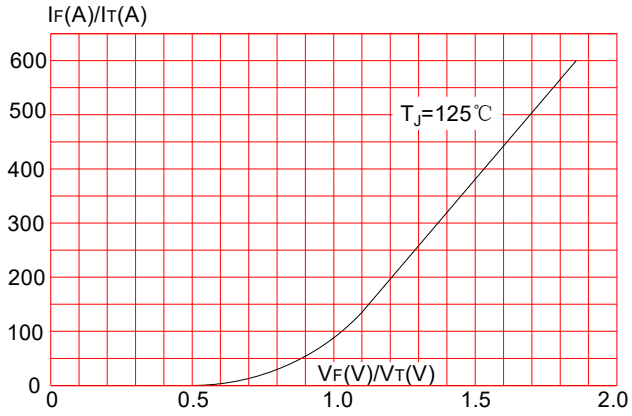


FIG.4: Relative variations of gate trigger current, holding current and latching current versus junction temperature